10-04-00

4.

JC893 U.S. PTO
10/02/00

SMITH, DANAMRAJ & YOUST

A PROFESSIONAL CORPORATION

ATTORNEYS AND COUNSELORS
INTELLECTUAL PROPERTY LAW AND RELATED MATTERS

STEVEN W SMITH
SHREEN K DANAMRAJ
LAWRENCE R YOUST

12900 PRESTON ROAD, SUITE 1200, LB 15
DALLAS, TEXAS 75230-1328

TELEPHONE (972) 720-1202
FAX (972) 720-1139

WRITER'S DIRECT DIAL NUMBER
(972) 392-2696

WRITER'S EMAIL ADDRESS
lawrence@sdylaw com

JC882 U.S. PTO
09/678163
10/02/00

October 2, 2000

Via Express Mail No.: EL593939936US

Box: Patent Applications
Commissioner for Patents
Washington, D.C. 20231

Re: Method for Selecting Components for a Matched Set From a Wafer Interposer Assembly
Attorney Docket No.: 1303-1008

Dear Sir:

Enclosed for filing please find the following items relating to the above-identified application:

(1) Original Patent Application with Formal Drawings;

(2) Declaration and Power of Attorney;

(3) Assignment with Cover Sheet;

(4) Fee Calculation Cover Sheet;

(5) Verified Statement Claiming Small Entity Status;

(6) Checks in the amount of $492.00, $92.00 and $40.00; and

(7) Post Card.

Please file the above and return the date-stamped postcard to our office at the address listed above. In the meantime, if you have any questions or comments concerning this matter, please call the undersigned at your earliest convenience. Otherwise, please accept the enclosed.

Sincerely,

Lawrence Youst

Lawrence R. Youst
Reg. No. 38,795

Enclosures

09678163 . 100200

Attorney Docket No. 1303-1008

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application: Jerry D. Kline

Serial No. Unknown

Filed: September 29, 2000

Art Unit: Unknown

Examiner: Unknown

For: Method for Selecting Components for a Matched Set From a Wafer Interposer Assembly

Commissioner for Patents
Washington, D.C. 20231

FEE CALCULATION

	NUMBER		NUMBER EXTRA	RATE	BASIC FEE $ 710.00
Total Claims	41	- 20 =	21	x $18=	$ 378.00
Independent Claims	4	- 3 =	1	x $80 =	$ 80.00
				Total of Above	$1168.00
				Reduction by 50% for filing by small entity	($584.00)
				TOTAL FEES	$584.00

The Commissioner is hereby authorized to charge any additional filing fee or credit any over payment to Deposit Account No.: 03-1130. All correspondence related to this application may be addressed to the undersigned at Smith, Danamraj & Youst, P.C., 12900 Preston Road, Suite 1200, LB-15, Dallas, Texas 75230.

Dated this 2nd day of October, 2000

Lawrence R. Youst
Attorney for Applicant(s)
Reg. No. 38,795

Date of Deposit October 2, 2000
"EXPRESS MAIL" mailing label number **EL593939936US**
I certify that the accompanying Patent Application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box Patent Application; Commissioner for Patents, Washington, DC 20231

Lawrence R Youst

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS - SMALL BUSINESS CONCERN

Applicant: Micro-ASI, Inc.

For: Method for Selecting Components for a Matched Set From a Wafer Interposer Assembly

I hereby declare that I am an official of the small business empowered to act on behalf of the concern identified below:

Name of Organization: Micro-ASI, Inc.

Address of Organization: 12655 North Central Expressway
Suite 1000
Dallas, Texas 75243

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1 27 (c)) - SMALL BUSINESS CONCERN

The type of organization is a small business concern.

I hereby declare that the organization identified above qualifies as a small business as defined in 37 C.F.R. §1.9(d), and thus is a "small entity" as defined in §1.9(f), for purposes of paying reduced fees under Sections 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that exclusive rights to the invention have been conveyed to and remain with the organization with respect to the invention, entitled "Chip Assembly with Integrated Power Distribution Between a Wafer Interposer and an Integrated Circuit Chip" by inventor Jerry D. Kline described in:

[X] the specification filed herewith
[ ] application serial no. ________________, filed ______________________.
[ ] patent no. ____________________, issued ________________________.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 C.F.R. 1.9(d) or a nonprofit organization under 37 C.F.R. 1.9(e).

> * NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities.

I acknowledge the duty to file, in this application or patent notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of person signing: Jerry D. Kline
Title of person other than owner: Vice President
Address of person signing: 1012 Remington Court, Argyle, Texas 76226

Signature: Jerry D. Kline Date: 9/29/00

Attorney Docket No.: 1303-1008

METHOD FOR SELECTING COMPONENTS FOR A MATCHED SET FROM A WAFER-INTERPOSER ASSEMBLY

TECHNICAL FIELD OF THE INVENTION

The present invention relates in general to integrated circuits and, more particularly, to wafer level testing of chips from a wafer that is coupled to an interposer for the selection of components for a matched set.

BACKGROUND OF THE INVENTION

Modern electronic devices utilize semiconductor chips, commonly referred to as integrated circuits, which incorporate numerous electronic elements. These chips are mounted on substrates which physically support the chips and electrically interconnect the chips with other elements of the circuit. Such substrates may then be secured to an external circuit board or chassis.

The size of the chips and substrate assembly is a major concern in modern electronic product design. The size of each subassembly influences the size of the overall electronic device. Moreover, the size of each subassembly controls the required distance between each chip and between chips and other elements of the circuit. Delays in transmission of electrical signals between chips are directly related to these distances. These delays limit the speed of operation of the device. Thus, more compact interconnection assemblies, with smaller distances between chips and smaller signal transmission delays, can permit faster operations.

One approach for improving overall system performance is through the use of matched sets. For example, several identical or dissimilar components that have been identified by the individual testing phase of component processing to have certain performance tracking characteristics may be

assembled together as a matched set. The components of such a matched sets are frequently attached to a single substrate in close proximity to one another. This strategy improves performance compared to conventional or non-optimized systems by reducing the overall space needed to accommodate the chips and by, among other things, shortening the distance between chips. Specifically, interconnect inductance and signal transmission delays are all reduced.

One type of matched set includes a collection of identical components which have been identified to meet specific system performance requirements. For example, radio frequency (RF) systems often employ identical filters, switches, power dividers, mixers and high frequency amplifiers. Typically, each of the identical components has been extensively tested individually prior to inclusion in this type of system. The individual characterization tests for a filter, for instance, might measure insertion loss and phase shift as a function of frequency, input power and temperature. These multi-dimensional arrays of data are then compared to each other to identify individual components that perform within acceptable limits relative to each other. Components that are found to exhibit similar behavior under the various input stimuli will constitute a matched set of identical devices. Conversely, components that are found to

exhibit dissimilar behavior under the various input stimuli, for example, the gain of one component having a negative slope over temperature while the gain of another component having a positive slope over temperature, will constitute a mismatch of components that will not be placed in a chip collection.

It has been found, however, the certain mismatches are not identified when the components are tested individually. In fact, certain mismatches are not identified until the entire chip collection is assembled and the components are tested together for the first time. As such, some chip collections must be disassembled so that the valuable components may be, for example, packaged as individual components, while other chip collections are simple discarded.

Therefore, a need has arisen for an improved method for selection of system components for a matched set. A need has also arisen for such a method that does not require elaborate data reduction of test results from individually tested components. Additionally, a need has arisen for such a method that allows for testing of the individual components together prior to the assembly of the matched set.

SUMMARY OF THE INVENTION

The present invention disclosed herein provides a chip collection, known as a matched set, that maximizes system performance by selecting well matched integrated circuit chips for assembly together into the matched set. The present invention achieves this result by allowing for testing of the various integrated circuit chips together prior to the assembly of the matched set. This testing is performed by connecting a wafer level interposer and a wafer to a testing apparatus. Thus, all of the chips to be included in the matched set may be tested together. After testing, the wafer-interposer assembly is diced into a plurality of chip assemblies that are assembled into the matched set.

In its broadest form, the present invention provides for the attachment of a semiconductor wafer having a plurality of integrated circuit chips thereon to an interposer for testing of the integrated circuit chips. The integrated circuit chips of the wafer may be, for example, DRAM chips, SRAM chips, amplifiers, controllers, converters or other devices that are commonly assembled in sets. Likewise, the integrated circuit chips of the wafer may be designed to carry any type of signal such as an analog signals, a digital signal, an RF signal or a mixed signal and the like.

Prior to testing, the wafer is electrically and mechanically coupling to the interposer such that the wafer-interposer assembly may be connected to a testing apparatus. The testing may include performance tests over a range of temperatures, including burn-in testing, vibration testing, testing for leakage currents, testing for offset voltages, testing for gain tracking, testing for bandwidth and the like to determine which integrated circuit chips from the wafer could be included in a matched set with other integrated circuit chips from that wafer to achieve optimum performance. Likewise, the testing may include grading of the integrated circuit chips for speed or other performance characteristics such that the integrated circuit chips that receive a particular grade are matched with other integrated circuit chips from that wafer having a similar grade. Additionally, the testing may include testing for non-conformance wherein certain integrated circuit chips may not be matched with any other integrated circuit chips from that wafer.

Once testing is complete, the wafer-interposer assembly may be diced into a plurality of chip assemblies. Two or more of these chip assemblies may them be matched with one another, for inclusion in a matched set. This selection is based upon the results of the testing of the integrated circuit chips. Using this process, all or substantially all of the integrated

circuit chips from the wafer may be matched with other integrated circuit chips from that wafer based upon the desired performance characteristics of the matched set that will contain these devices. By performing the testing prior to assembly of the matched set, the performance characteristics of each of the matched sets assembled using integrated circuit chips from the tested wafer is enhanced as is the overall performance of the entire lot of matched set devices.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the features and advantages of the present invention, reference is now made to the detailed description of the invention along with the accompanying figures in which corresponding numerals in the different figures refer to corresponding parts and in which:

Figure 1 is an exploded view of a wafer-interposer assembly of the present invention including a wafer having a plurality of chips;

Figure 2 is an exploded view of a wafer-interposer assembly of the present invention including a wafer having a plurality of chips;

Figures 3A-3B are cross sectional views taken respectively along line 3A-3A of Figure 1 and 3B-3B of figure 2;

Figure 4 is a partially exploded view of a wafer-interposer assembly of the present invention inserted into a testing apparatus;

Figure 5 is an exploded view of a wafer-interposer assemblies of the present invention;

Figure 6 is an isometric view of a plurality of chip assemblies after singulation of a wafer-interposer assembly of the present invention; and

Figure 7 is an isometric view of a matched set of chip assemblies of the present invention in place on a substrate;

DETAILED DESCRIPTION OF THE INVENTION

While the making and using of various embodiments of the present invention are discussed in detail below, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention and do not define the scope of the invention.

The general features of a wafer-interposer assembly of the present invention is shown in figure 1 and are generally designated 10. Wafer-interposer assembly 10 includes a wafer interposer 12, an array 14 of conductive attachment elements 16 and a wafer 18. Interposer 12 has an array 20 of conductive contact pads 22 on the upper surface thereof. Array 20 is split into sixteen sections separated by dotted lines. The dotted lines represent the locations where interposer 12 will be cut when interposer 12 is diced into chip assemblies, including a section of interposer 12 and an associated chip from wafer 18, as will be described in more detail below. It should be noted that while array 20 of interposer 12 is depicted as having sixteen sections in figure 1, this depiction is for simplicity and clarity of description as those skilled in the art will recognize that actual

interposers will have several hundred or several thousand sections which correspond to the several hundred or several thousand chips on typical wafers.

Each of the sixteen sections of array 20 has sixteen contact pads 22 depicted therein. The contact pads 22 represent the locations where interposer 12 will be electrically connected to a substrate once interposer 12 has been diced into chip assemblies, as will be described in more detail below. It should be noted that while array 20 is depicted as having sixteen contact pads 22 in each section in figure 1, this depiction is for simplicity and clarity of description as those skilled in the art will recognize that the actual number of contact pads 22 in each section will be several hundred or several thousand contact pads.

On the lower surface of interposer 12 there is an array of conductive contact pads (not pictured). In the illustrated embodiment, the contact pads on the lower surface of interposer 12 have the same geometry as contact pads 22. The contact pads on the lower surface of interposer 12 represent the locations where interposer 12 will be electrically connected to wafer 18, as will be described in more detail below. It should be noted that directional terms, such as above, below, upper, lower, etc., are used for convenience in referring to the accompanying drawings as it is to be

understood that the various embodiments of the present invention described herein may be utilized in various orientations, such as inclined, inverted, horizontal, vertical, etc., without departing from the principles of the present invention.

Array 14 of conductive attachment elements 16 is split into sixteen sections separated by dotted lines. Each of the sections has sixteen conductive attachment elements 16 that correspond to the contact pads on the lower surface of interposer 12. Conductive attachment elements 16 may be in the shape of balls, bumps, columns and the like. Conductive attachment elements 16 may be formed from any suitable electrically conductive material such as solder, including tin based solder, gold based solder, zinc based solder, indium based solder and the like. Alternatively, conductive attachment elements 16 may be formed from a conductive epoxy, a conductive polymer or the like. Conductive attachment elements 16 may be attached to interposer 12 by any number of attachment techniques including screening, flowing, molding, reflowing, dipping, electroplating, adhering and the like, depending upon which material is used for conductive attachment elements 16.

Wafer 18 has a plurality of chips 24 depicted thereon having dotted lines therebetween that represent the locations

where wafer 18 will be cut when wafer 18 is diced into chip assemblies, as will be described in more detail below. Wafer 18 is depicted as having sixteen chips 24. This depiction is for simplicity and clarity of description as those skilled in the art will recognize that actual number of chips 24 on wafer 18 will be several hundred or several thousand.

Each chip 24 has a plurality of conductive contact pads 26 on its face. Each chip 24 is depicted as having sixteen contact pads 26, for simplicity and clarity of description, which correspond with one of the conductive attachment elements 16 in array 14 and represent the locations where chips 24 will be electrically connected to interposer 12. It should be noted by those skilled in the art that the actual number of contact pads 26 on each chip 24 will be several hundred or several thousand instead of sixteen.

After assembly, conductive attachment elements 16 of array 14 electrically connect and mechanically bond contact pads 26 of each chip 24 to the facing contact pads on the lower surface of interposer 12. These permanent electrical and mechanical connections may be achieved using, for example, a heating method such as reflowing or thermal compression.

Wafer-interposer assembly 10 allows for the simultaneous testing of groups of chips 24 or all of the chips 24 of wafer 18. Simultaneous testing provides added efficiency to the

testing process as numerous aspects of the functionality and performance of chips 24 may be tested. Importantly, this type of simultaneous testing allows for a determination of which chips 24 match up best with one another. This allows for optimization of the overall performance of specific matched sets as well as the overall performance of all the matched sets made from chips 24. In this embodiment, the matched sets will comprise two or more chips 24. For example, these matched sets may include multiple SRAM or DRAM components for use in a digital device, multiple amplifiers components for use in an analog device, multiple mixer, atteruator or circulator components for a RF device, multiple converter components for a mixed signal device and the like.

Referring now to figure 2, therein is depicted a wafer-interposer assembly 30 of the present invention. Wafer-interposer assembly 30 includes a wafer interposer 32, an array 34 of conductive attachment elements 36 and a wafer 38. Interposer 32 has an array 40 of conductive contact pads 42 on the upper surface thereof. Array 40 is each split into sixteen sections separated by dotted lines which represent the locations where interposer 32 will be diced.

Each of the sixteen sections of array 40 has sixteen contact pads 42 depicted therein. The contact pads 42 represent the locations where interposer 32 will be

electrically connected to a substrate once interposer 32 has been diced. On the lower surface of interposer 32 there is an array of conductive contact pads (not picture). In the illustrated embodiment, the contact pads on the lower surface of interposer 32 do not have the same geometry as contact pads 42, as will be explained in greater detail below.

Array 34 of conductive attachment elements 36 is split into sixteen sections separated by dotted lines. Each of the sections has thirty-six conductive attachment elements 36 that correspond to the contact pads on the lower surface of interposer 32.

Wafer 38 has a plurality of chips 44 depicted thereon having dotted lines therebetween that represent the locations where wafer 38 will be diced. Wafer 38 is depicted as having sixteen chips 44. Each chip 44 has a plurality of conductive contact pads 46 on its face. Each chip 44 is depicted as having thirty-six contact pads 46, which correspond with the conductive attachment elements 36 in array 34 and represent the locations where chips 44 will be electrically connected to interposer 32.

Referring next to figure 3A a cross sectional view of interposer 12 taken along line 3A-3A of figure 1 is depicted. Interposer 12 includes a plurality of layers having routing lines and vias therein which serve as electrical conductors.

One set of conductors, depicted as conductors 50, 52, 54 and 56, pass through interposer 12 and serve to electrically connect pads 26 of chips 24 to the contact pads 22 of interposer 12. These conductors are selected to have suitable conductivity and may be, for example, aluminum or copper. Interposer 12 also includes a set of testing conductors, depicted as conductor 58, that pass through interposer 12 connecting some of the contact pads 26 of chips 24 to a testing apparatus as will be explained in greater detail below. The testing conductors may provide direct electrical connection to the testing apparatus or may pass through a multiplexer or other intervening apparatus (not shown) incorporated into interposer 12.

It can be seen that contact pads 26 of chips 24 and contact pads 22 of interposer 12 have identical geometries. The present invention, however, is by no means limited to having identical geometries. As each die design may have unique pad geometry, one of the advantages of the present invention is that the contact pads on the upper surface of an interposer may utilize a geometry that is different from that of the contact pads of the chips. Traditionally, chip designers have been limited in chip layout in that all of the I/O of a chip had to be made either through the peripheral edges of the chip (for wire bonding) or at least through a

standard pin or pad layout defined by a standardization body, such as the Joint Electrical Dimensional Electronic Committee (JEDEC). The interconnection requirements, therefore, have traditionally driven the chip layout. Chip designs for use with an interposer of the present invention are not limited by such constraints.

For example, as best seen in figure 3B, interposer 32 includes a plurality of layers having routing lines and vias therein which serve as electrical conductors. One set of conductors, depicted as conductors 60, 62, 64 and 66 pass through interposer 32 to electrically connect contact pads 42 on the upper surface of interposer 32 to contact pads 46 on chips 44 (see figure 2). Another set of conductors, depicted as conductors 68 and 70, are testing conductors that pass through interposer 32 and are used to connect certain pads 46 of chips 44 (see figure 2) to a testing apparatus, as will be explained in greater detail below. As such, the geometry of pads 42 on the upper surface of interposer 32 is different from that of pads 46 on chips 44.

Referring now to figure 4, therein is depicted a wafer-interposer assembly 80 connected to a testing unit 82. Wafer-interposer assembly 80 includes a wafer interposer 84 and a wafer 92. Wafer-interposer assembly 80 interfaces with testing unit 82 through a testing connector 88 that comprises

a plurality of testing contacts 90, shown here as pins. The testing contacts 90 of testing connector 88 connect with the testing sockets of testing connector 86 of wafer-interposer assembly 80.

After electrical connection to the testing unit 82, wafer-interposer assembly 80 can be used to run the chips on wafer 92 through any number of tests including a complete parametric test, a burn-in or whatever subsets thereof are deemed necessary for that particular chip design. During the course of testing, signals may be sent to individual chips, groups of chips or all of the chips to test each function of the chips which may ideally occur across a range of conditions, so as to simulate real world operation. Testing unit 82 may incorporate a heating and cooling apparatus for testing the chips across a range of temperatures including burn-in testing. Testing unit 82 may also incorporate a device for vibrating or otherwise mechanically stressing the chips.

More specifically, wafer-interposer assemblies 80 of the present invention may be used to select chips from wafer 92 that will be used in a matched set of chips. For example, the testing may include performance tests over a range of temperatures, testing for leakage currents, testing for offset voltages, gain tracking, bandwidth and the like to determine

which of the chips from wafer 92 could be included in a matched set with other chips from wafer 92 to achieve optimum performance. Alternatively, the testing may result in giving each of the chips a grade for speed or other performance characteristics such that chips of a particular grade may be matched with other chips of that same grade. Additionally, the testing may result in a non-conformance or mismatch determination wherein certain chips may not be matched with certain other chips. Certain chips may alternatively be designated as incompatible with any other chips.

Referring next to figure 5, a wafer-interposer assembly 100 is depicted including a wafer-interposer 102 and a wafer 104. Wafer-interposer assembly 100 also includes an array 106 of conductive attachment elements 108. Array 106 is split into sixteen sections separated by dotted lines. Each of the sections has sixteen conductive attachment elements 108 that correspond to contact pads 110 of array 112 on interposer 102.

After assembly, conductive attachment elements 108 will be used to electrically connect and mechanically bond a diced section of wafer-interposer assembly 100, including a section of interposer 102 and its associated chip from wafer 104 to a substrate, as will be explained in more detail below. These permanent electrical and mechanical connections may be

achieved using, for example, a heating method such as reflowing or thermal compression.

Figure 6 shows an array 120 of chip assemblies 122 after singulation of a wafer-interposer assembly of the present invention. Each chip assembly 122 comprises a chip 124 from a wafer, a section 126 of an interposer and a plurality of conductive attachment elements 128 disposed on conductive contact pads 130 on the exposed surface of chip assemblies 122. Once chip assemblies 122 have been singulated, chip assemblies 122 may be sorted based upon the testing performed at the wafer level. For example, if chips 124 of chip assemblies 122 are filters for a radio frequency (RF) systems, the testing might have measured parameters such as insertion loss and phase shift as a function of the frequency, the input power and the temperature. The various chips 124 of chip assemblies 122 that are found to exhibit similar behavior when tested together may now be selected for inclusion in a matched set. Conversely, various chips 124 of chip assemblies 122 that are found to exhibit dissimilar or incompatible behavior when tested together will not be included in a matched set.

As will be understood by those skilled in the art, depending upon the type of components and the desired service to be performed by the matched set, an appropriate testing regiment will be designed to test the functionality of chips

124 that is critical to the desired performance of a matched set including chips 124. For example, the testing regiment may be designed to identify which chips 124 perform best together to allow for the assembly of high performance matched sets using high performing groups of chips 124, i.e., two or more chips 124, thereby maximizing the performance of a selected number of matched sets assembled from chip assemblies 122. Alternatively, a testing regiment may be designed to result in the grading of the performance of groups of chips 124 when tested together such that the performance of the lot of matched sets assembled using chip assemblies 122 may be maximized. As yet another alternative, a testing regiment may be designed to result in a finding of which chips 124 are compatible with each other such that those chips 124 may be included together as components in a matched set and which chips 124 are incompatible with each other and should not be included together as components in a matched set. Additionally, such a test regiment may identify certain chips 124 as being incompatible with any other chips 124 and should not be included in any matched set. Additionally, it should be noted by those skilled in the art that any effects of the interposer on the testing of the chips are inherently taken into account during testing as the interposer and the wafer are diced together such that a section of the interposer and

a chip remain together as will be explained in greater detail below.

As best seen in figure 7, several chip assemblies 122 may be mounted together on a substrate 132 as a matched set. Substrate 132 has a plurality of conductive layers 134 and dielectric layers 136. Chip assemblies 122 are electrically and mechanically attached to contact pads on the surface of substrate 132 through conductive attachment elements 128. Assembled as shown, the diced sections 126 of the interposer provide electrical connection between chips 124 and substrate 132. In certain embodiments, substrate 132 may be a traditional FR4 circuit board. Alternatively, substrate 132 may be composed of a higher grade material such as a ceramic, which is typically used in multichip packages.

While figure 7 has depicted a matched set of component as including four chip assemblies 122, it should be understood by those skilled in the art that any number of chip assemblies may be utilized in such a matched set. The specific number of chip assemblies will be selected based upon the desired functionality of the matched set. The testing process of the present invention provides for each of the components of a matched set, regardless of the number, to be tested together as part of a single testing procedure. As such, the

components for the matched sets are selected for assembly only after successful testing.

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

What is claimed is:

1. A method for selecting components for a matched set comprising the steps of:

electrically and mechanically coupling a semiconductor wafer having a plurality of integrated circuit chips to an interposer to form a wafer-interposer assembly;

testing the integrated circuit chips of the semiconductor wafer;

dicing the wafer-interposer assembly into a plurality of chip assemblies; and

selecting at least two of the chip assemblies for inclusion in the matched set based upon the testing.

2. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify which groups of integrated circuit chips perform best together for inclusion in a selected number of high performance matched sets.

3. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing groups of integrated circuit chips together to grade the groups of integrated circuit chips for performance such that the overall performance of matched sets assembled from the chip assemblies is maximized.

4. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify the compatibility of individual integrated circuit chips with one another.

5. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify which individual integrated circuit chips are incompatible with one another.

6. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for performance over a range of temperatures.

7. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises performing burn-in testing of the integrated circuit chips.

8. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises vibrating the integrated circuit chips.

9. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for leakage currents.

10. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for offset voltages.

11. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for gain tracking.

12. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for bandwidth.

13. The method as recited in claim 1 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for speed grades.

14. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are digital devices.

15. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are analog devices.

16. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are RF devices.

17. The method as recited in claim 1 wherein the integrated circuit chips of the semiconductor wafer are mixed signal devices.

18. A method for assembling a matched set comprising the steps of:

providing a semiconductor wafer having a plurality of integrated circuit chips;

electrically and mechanically coupling the wafer to an interposer to form a wafer-interposer assembly;

testing the integrated circuit chips of the wafer;

dicing the wafer-interposer assembly into a plurality of chip assemblies;

sorting the chip assemblies based upon the testing; and

electrically coupling at least two of the chip assemblies onto a substrate, thereby assembling the matched set.

19. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify which groups of integrated circuit chips perform best together for inclusion in a selected number of high performance matched sets.

20. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing groups of integrated circuit chips together to grade the groups of integrated circuit chips for performance such that the overall performance of matched sets assembled from the chip assemblies is maximized.

21. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify the compatibility of individual integrated circuit chips with one another.

22. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing groups of the integrated circuit chips together to identify which individual integrated circuit chips are incompatible with one another.

23. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for performance over a range of temperatures.

24. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises performing burn-in testing of the integrated circuit chips.

25. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises vibrating the integrated circuit chips.

26. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for leakage currents.

27. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for offset voltages.

28. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for gain tracking.

29. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for bandwidth.

30. The method as recited in claim 18 wherein the step of testing the integrated circuit chips further comprises testing the integrated circuit chips for speed grades.

31. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer are digital devices.

32. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer analog devices.

33. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer mixed signal devices.

34. The method as recited in claim 18 wherein the integrated circuit chips of the semiconductor wafer are RF devices.

35. A matched set assembled by the method as recited in claim 18.

36. A matched set of integrated circuit chips including at least two integrated circuit chips from wafer, the integrated circuit chips being tested together as part of a wafer-interposer assembly including the wafer and a wafer interposer, the matched set comprising:

a first chip assembly diced from the wafer-interposer assembly;

a second chip assembly diced from the wafer-interposer assembly; and

a substrate on to which the first and second chip assemblies are electrically coupled.

37. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are digital devices.

38. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are analog devices.

39. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are RF devices.

40. The matched set as recited in claim 36 wherein the integrated circuit chips of the semiconductor wafer are mixed signal devices.

41. The matched set as recited in claim 36 further comprising a third chip assembly diced from the wafer-interposer assembly, the third chip assembly electrically coupled to the substrate.

METHOD FOR SELECTING COMPONENTS FOR A MATCHED SET FROM A WAFER-INTERPOSER ASSEMBLY

ABSTRACT OF THE DISCLOSURE

A matched set of integrated circuit chips (24) and a method for assembling such integrated circuit chips (24) into a matched set are disclosed. A semiconductor wafer (18) having a plurality of integrated circuit chips (24) is electrically and mechanically coupled to a wafer interposer (12) to form a wafer-interposer assembly (10). The integrated circuit chips (24) of the wafer (18) are then testec together by attaching the wafer-interposer assembly (10) to a testing apparatus and running the integrated circuit chips (24) through various testing sequences. The wafer-interposer assembly (10) is then diced into a plurality of chip assemblies each having a chip (24) and a section of the wafer interposer (12). Based upon the testing, the chip assemblies are sorted and at least two of the chip assemblies are selected for inclusion in the matched set.

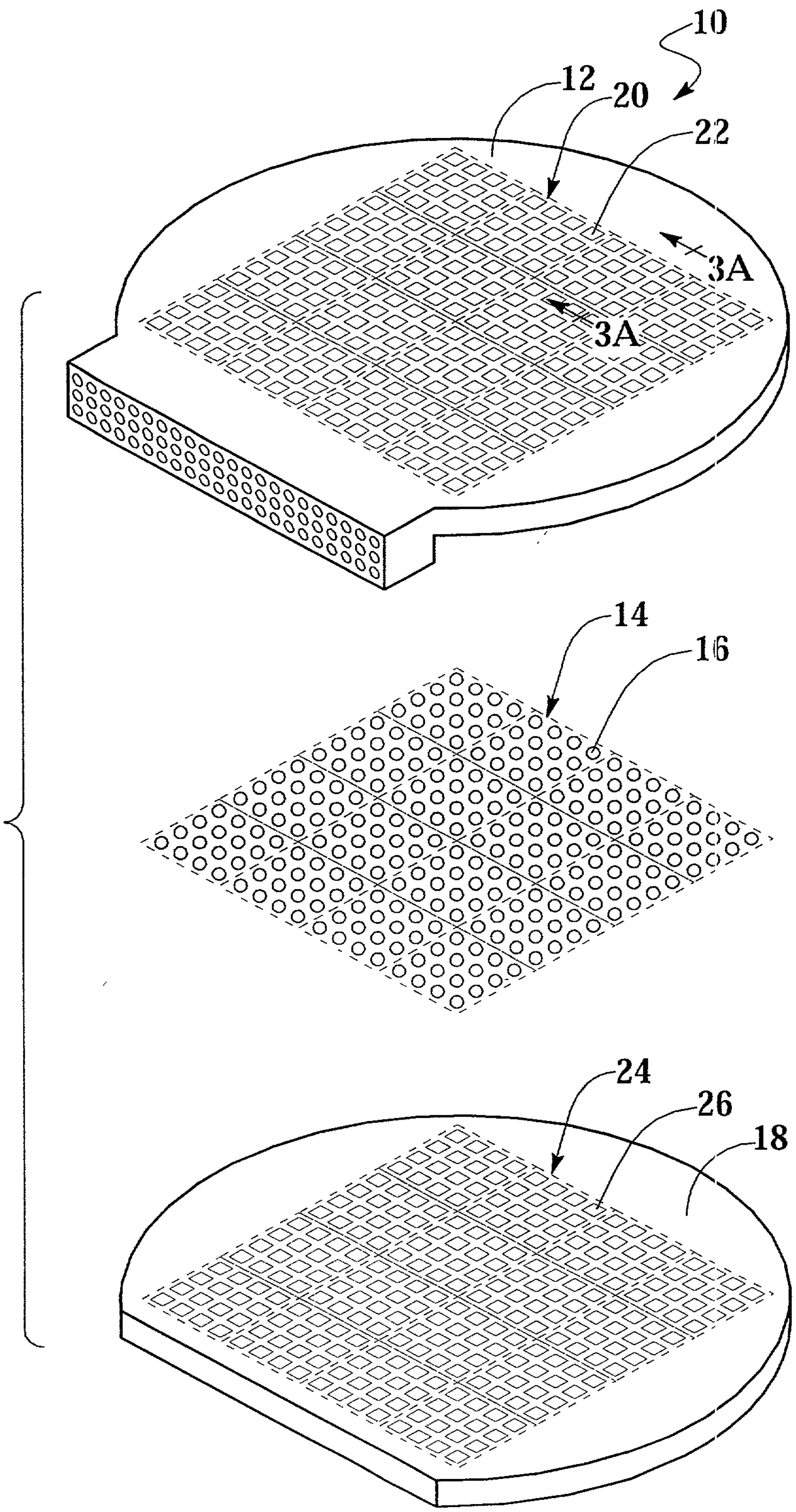


Fig.1

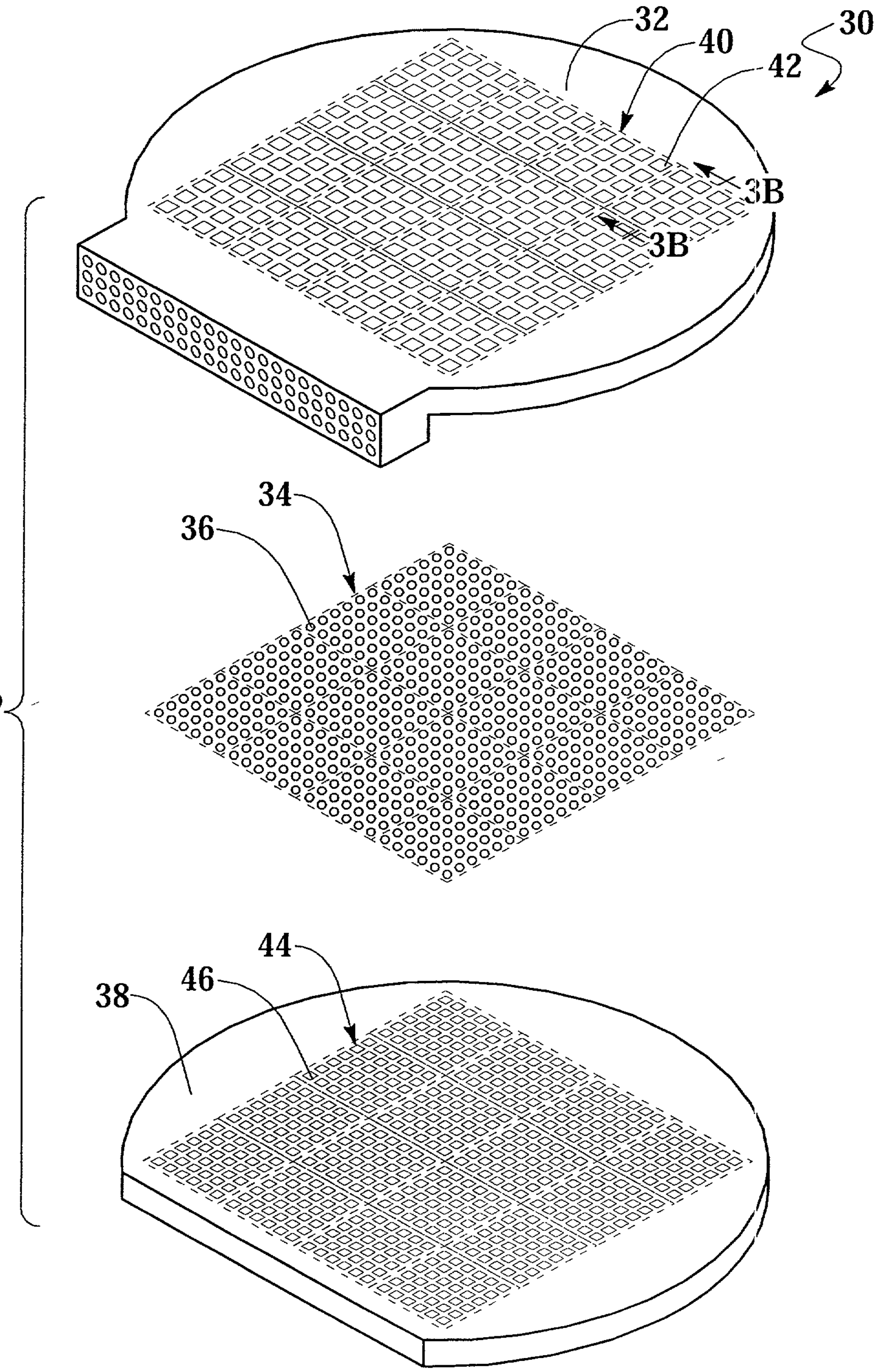
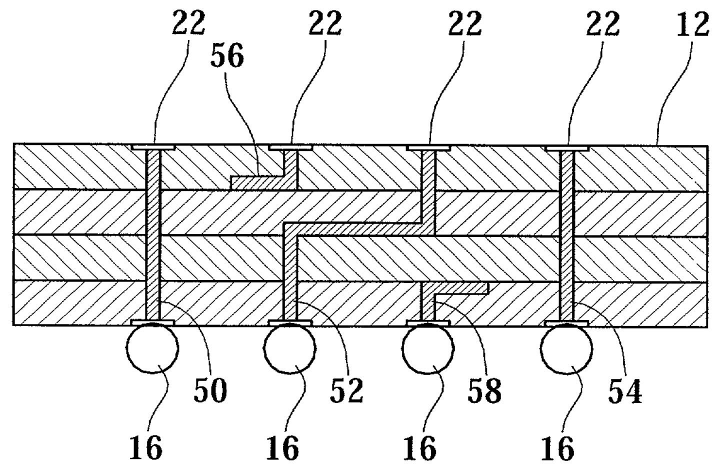
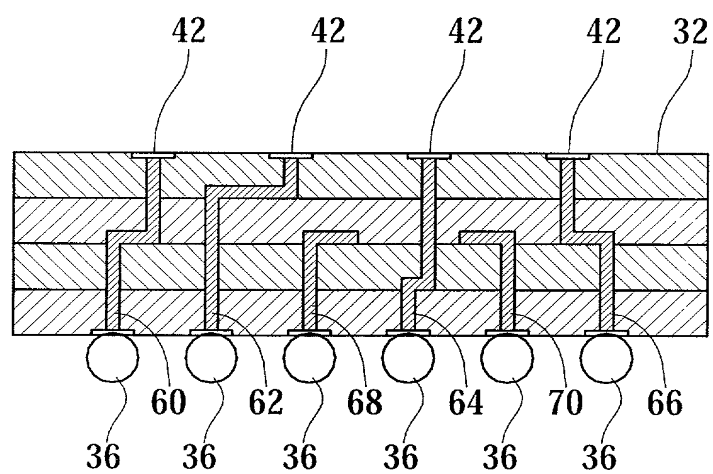


Fig.2


22
56
22
22
22
12
50
52
58
54
16
16
16
16
Fig.3A


42
42
42
42
32
60
62
68
64
70
66
36
36
36
36
36
36
Fig.3B

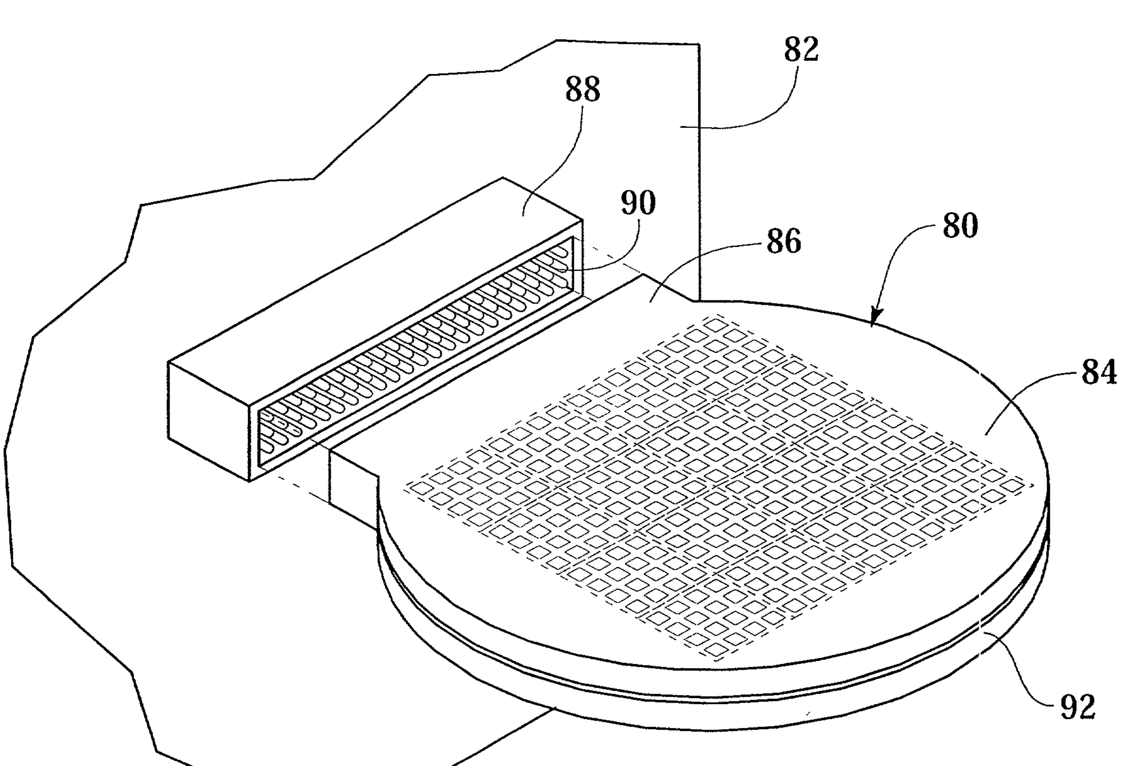


Fig.4

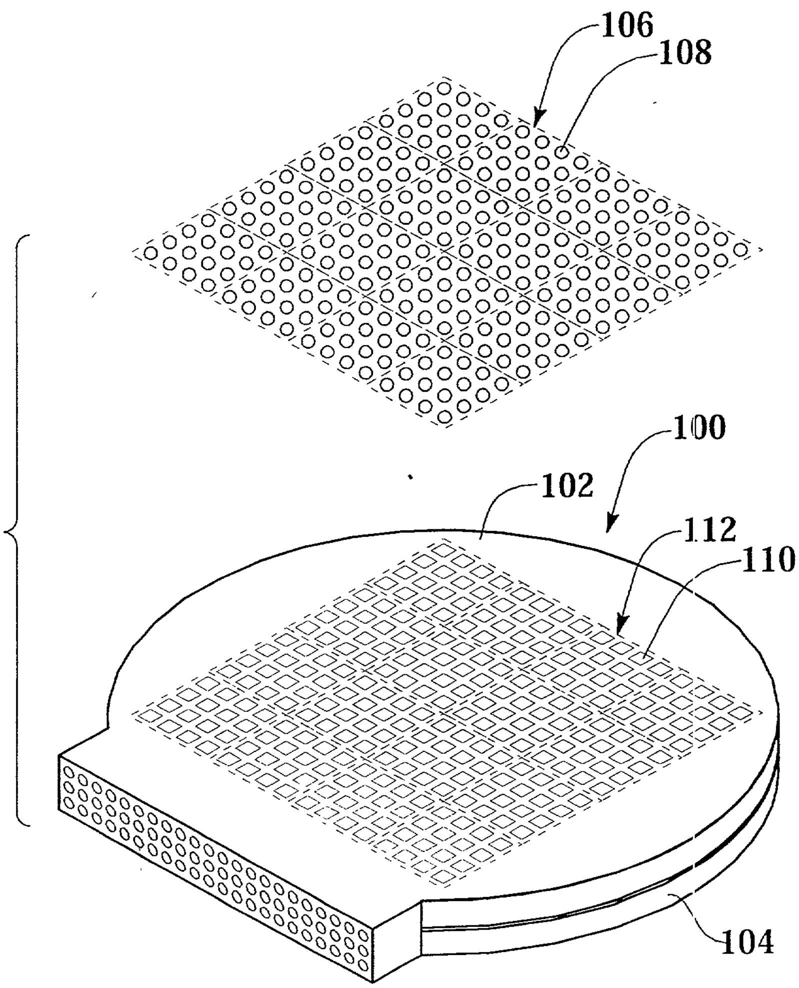
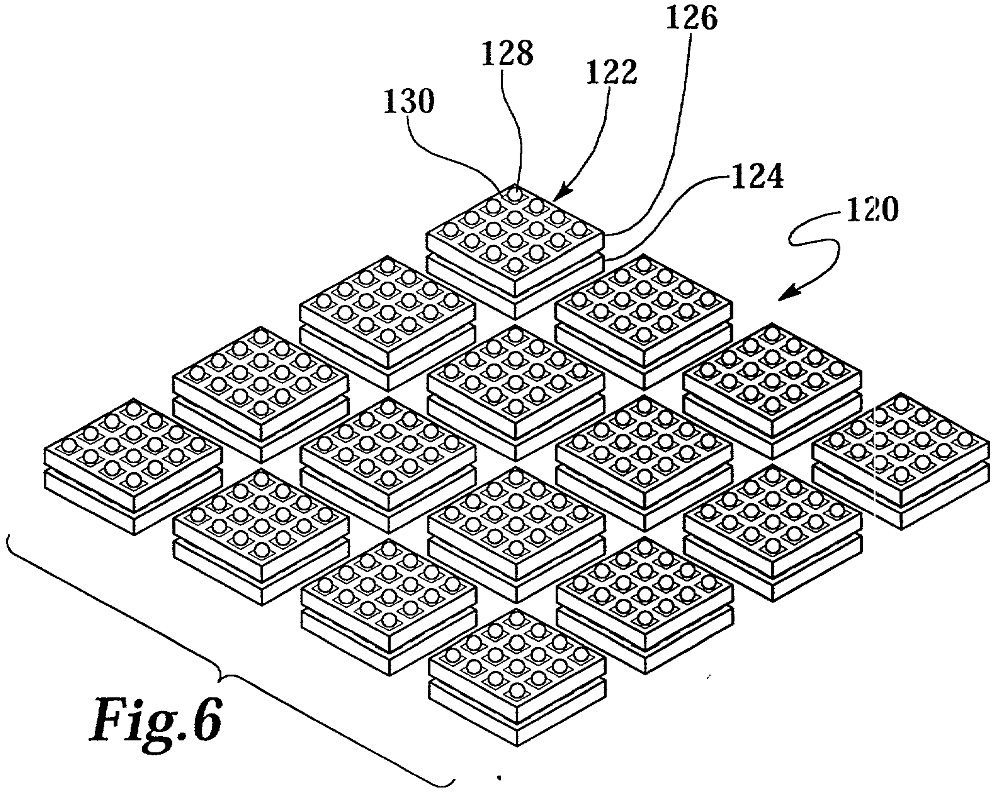
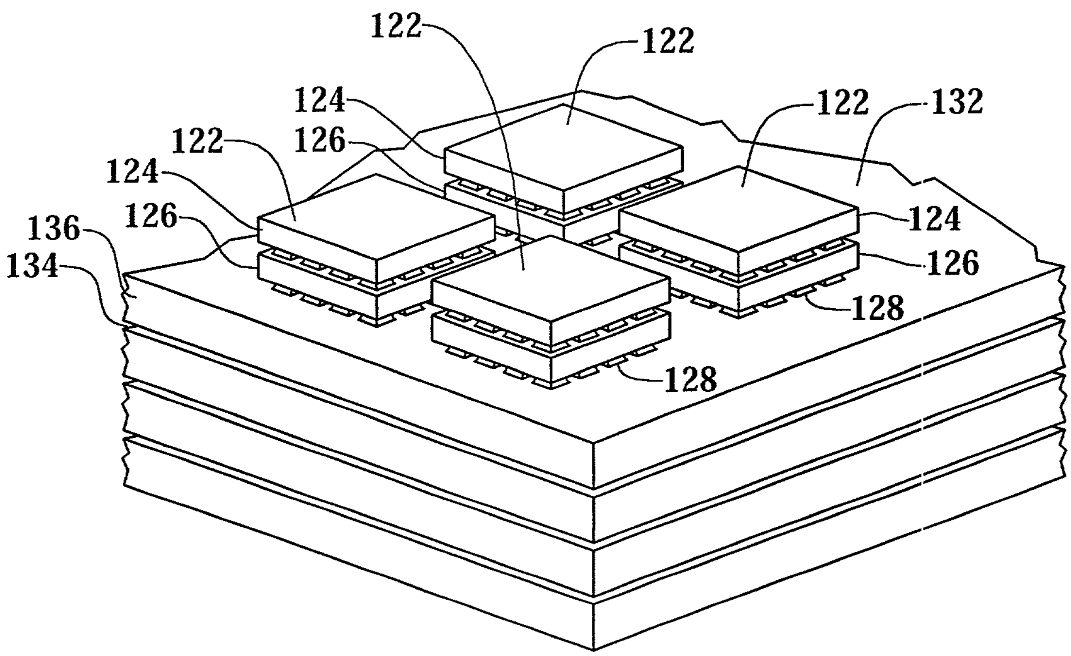


Fig.5



126
128
122
130
124
120

Fig.6



122
122
124
122
132
122
126
124
126
124
136
126
126
134
128
128

Fig.7

Attorney Docket No.: 1303-1008

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

This declaration is of the following type: (check one)

(X) Original
( ) Design
( ) Supplemental
( ) National Stage of PCT

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Method for Selecting Components for a Matched Set From a Wafer Interposer Assembly

the specification of which: (check one)

(X) is attached hereto;
( ) was filed on , as Application Serial No. , and was amended on (if applicable);
( ) was described and claimed in PCT International Application No. filed on and amended under PCT Article 19 on (if any).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a), and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a patent.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application of which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

Number	Country	Day/Month/Year Filed	Priority Claimed

This declaration is of the following type: (if applicable)

( ) Divisional
( ) Continuation
( ) Continuation-in-part

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States Application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, we hereby acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) jointly and severally to prosecute this application and transact all business in the Patent and Trademark Office connected therewith and to file any and all International Application(s) with respect thereto and to act on my behalf before the competent International Authorities with respect thereto: Lawrence R. Youst (Reg. No. 38,795); Steven W. Smith (Reg. No. 36,684) and Shreen K. Danamraj (Reg. No. 41,696) of Smith, Danamraj & Youst, P.C., 12900 Preston Road, Suite 1200, LB 15, Dallas, Texas 75230-1328.

SEND CORRESPONDENCE TO:

Lawrence R. Youst
Smith, Danamraj & Youst, P.C.
12900 Preston Road
Suite 1200, LB 15
Dallas, TX 75230-1328

DIRECT TELEPHONE CALLS TO:

Lawrence R. Youst
(972) 392-2696
(972) 720-1139 (FAX)

I hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1	Jerry D. Kline **Full Name**	Jerry D. Kline **Inventor's Signature**	9/29/00 **Date**
	1012 Remington Court Argyle, Texas 76226 **Residence**		U.S.A. **Citizenship**
	1012 Remington Court Argyle, Texas 76226 **Post Office Address**		